WHAT IS CLAIMED IS:

1. A method of forming a retrograde well in a transistor, comprising:

forming a transistor structure having a substrate, a gate, and a gate oxide layer between the substrate and the gate, the substrate including a channel region located generally below the gate;

implanting a first dopant into the channel region;

implanting a second dopant into the substrate to form a doped source region and a doped drain region;

implanting a third dopant into the gate oxide layer;

performing a source/drain anneal to form a source and a drain in the doped source region and the doped drain region, respectively, the source/drain anneal causing a portion of the first dopant in the channel region to be attracted by the third dopant into the gate oxide layer.

2. The method of Claim 1, wherein the transistor structure is an NMOS transistor structure.

3. The method of Claim 1, wherein implanting a first dopant into the channel region comprises implanting a first dopant using at least one halo implant.

4. The method of Claim 3, wherein the first dopant comprises boron.

5. The method of Claim 4, wherein the first dopant comprises boron and the third dopant comprises hydrogen.

6. The method of Claim 1, wherein the third dopant comprises hydrogen.

7. The method of Claim 1, wherein the third dopant comprises deuterium.

8. The method of Claim 1, wherein the third dopant comprises phosphine (PH_3).

9. The method of Claim 1, wherein implanting a third dopant into the gate oxide layer comprises implanting a third dopant into the gate such that a portion of the third dopant is communicated into the gate oxide layer.

10. The method of Claim 1, wherein the steps of implanting the second dopant and implanting the third dopant are performed at least partially simultaneously.

11. The method of Claim 1, further comprising forming a cap over the gate before performing the source/drain anneal such that the cap at least partially prevents the third dopant from escaping during the source/drain anneal.

12. The method of Claim 11, wherein the cap comprises nitride.

13. An integrated circuit comprising a plurality of transistors, a particular one of the transistors including a substrate, a gate, and a gate oxide layer between the substrate and the gate, the substrate including a channel region located generally below the gate;

wherein the channel region includes a retrograde well having been formed at least by:

implanting a first dopant into the channel region;

implanting a second dopant into the substrate to form a doped source region and a doped drain region;

implanting a third dopant into the gate oxide layer;

performing a source/drain anneal to form a source and a drain in the doped source region and the doped drain region, respectively, the source/drain anneal causing a portion of the first dopant in the channel region to be attracted by the third dopant into the gate oxide layer such that the concentration of the third dopant in the channel region increases from a first region adjacent the gate oxide layer to a second region further from the gate oxide.

14. The integrated circuit of Claim 13, wherein the particular transistor is an NMOS transistor.

15. The integrated circuit of Claim 13, the first dopant having been implanted into the channel region using at least one halo implant.

16. The integrated circuit of Claim 15, wherein the first dopant comprises boron.

17. The integrated circuit of Claim 16, wherein the first dopant comprises boron and the third dopant comprises hydrogen.

18. The integrated circuit of Claim 13, wherein the third dopant comprises hydrogen.

19. The integrated circuit of Claim 13, wherein the third dopant comprises deuterium.

20. The integrated circuit of Claim 13, wherein the third dopant comprises phosphine (PH_3).

21. The integrated circuit of Claim 13, the third dopant having been implanted into the gate such that a portion of the third dopant is communicated into the gate oxide layer.

22. The integrated circuit of Claim 13, the second dopant and the third dopant having been implanted at least partially simultaneously.

23. The integrated circuit of Claim 13, the retrograde well having been formed additionally by forming a cap over the gate before performing the source/drain anneal such that the cap at least partially prevents the third dopant from escaping during the source/drain anneal.

24. The integrated circuit of Claim 11, wherein the cap comprises nitride.

25. An integrated circuit comprising a plurality of transistors, a particular one of the transistors including a substrate, a gate, and a gate oxide layer between the substrate and the gate, the substrate including a channel region located generally below the gate, the channel region including a retrograde well of boron dopant.

26. The integrated circuit of Claim 25, wherein the concentration of boron in the retrograde well increases from a first region of the well adjacent the gate oxide layer to a second region of the well further from the gate oxide.

27. The integrated circuit of Claim 13, wherein the particular transistor is an NMOS transistor.